Ahmed Maroof

Electrical Engineer

I am a passionate engineering student with a strong academic background and good problem-solving skills. I am eager to apply my electrical background and further enhance my expertise in the realm of electrical research and innovation. Possess excellent communication skills and creativity. Flexible to do my role and have good management deftness too.

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EDUCATION

Electrical Engineering
Namal University Mianwali

10/2020 - Present *3.22/4.0*

Courses

- Computer Architechture
- Digital Logic Design
- Machine Learning
- Embedded Systems
- VLSI Design
- Computer Programming
- Digital Image Processing
- Wireless Communication

FSc Pre-Engineering
Govt. Postgraduate College Sahiwal

08/2018 - 07/2022 *Marks: 89%*

PERSONAL PROJECTS

Integration and Verification of L1 Data Cache in SweRV EH1 (11/2023 - Present)
- My final year project is about integrating L1 data cache in an open source RISC-V core by modifying the RTL in Systemverilog and then verifying using standard tools.

4-way Associative Data Cache
- Implementation of a 32KB, 4-way associative data cache with LRU (Least Recent Used) policy, using SystemVerilog.Performed simulation and verification via Iverilog and Verilator.

Pipelined RISCV Processor
- 5 stage pipelined RISCV based processor with the forwarding unit to handle data hazards.

Single Cycle RISCV Processor
- Designed complete RISCV based single cycle data path in Verilog for R, I, S, B type of instructions. Verified using test benches.

Obstacle Avoidance Robot
- A small robot capable of avoiding obstacles, using AVR microcontroller Atmega328p, instructed in C language, Embedded Systems

4-bit ALU at Hardware Level
- Implemented hardware(gate level) on breadboard and performed software(verilog) simulation using ModelSim, Digital logic Design

WORK EXPERIENCE

RTL Design and Linux Fundamental Intern
CESD Namal & 10xEngineers

07/2022 - 08/0222

Basic training

- Practiced verilog and systemverilog cadence-based exercises using the EDA tool to understand RTL design and verification in frontend VLSI design. I also exercised Ubuntu Linux fundamentals via My Missing CS Semester.

SKILLS

RTL Design and Verification | RISC-V | C | Python | Verilog | Systemverilog | MATLAB | Linux | Microarchitechture | Teamwork | Communication | Microsoft Office | RISCV Assembly | Verilator | Iverilog

ACHIEVEMENTS

IEEE Conference Paper
Our IEEE conference paper on "Integration and Verification of L1 Data Cache in SweRV EH1" has been accepted in ICECT 2024 for publication.

Full Merit Based Scholarship
I got a merit-based scholarship for my 4-year bachelor degree in electrical engineering at Namal University Mianwaly.

CO-CRICULLUM ACTIVITIES

IEEE Namal Student Branch
I volunteered to work as a graphics head..

Freelancer (01/2022 - Present)
I provide freelance service in graphic design and also in RTL design verification on Fiverr and Upwork.

CERTIFICATES

High Performance Computing and Parallel Programming Workshop
I participated in a workshop on HPC and parallel programming held by the Center of AI and Big Data at Namal University.

Verilog and Linux Fundamentals (07/2022 - 08/2022)
CESD Namal and 10xEngineers , awarded by this after training of 6 weeks

LANGUAGES

English
Professional Working Proficiency

Urdu
Native or Bilingual Proficiency

Punjabi
Full Professional Proficiency

INTERESTS

Computer Hardware | Robotics | Freelancing