Muhammad Attaullah Khan

Electrical Engineer

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Mianwali
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An ambitious and driven electrical engineering graduate with a passion for open source RISC-V technology. With a strong foundation in open source tools, embedded systems, FPGA Boards, computer architecture coupled with an interest in hardware description languages, I approach challenges with a creative and analytical mindset.

EDUCATION

Electrical Engineering
NamalUniversityMianwali

07/2020 - Present *3.69*

Courses

- Computer Architecture
- Embedded Systems
- Computer Communication Networks
- Digital Signal Processing
- Digital Logic Design
- Power Electronics
- Data Structures and Algorithms
- Basic Circuit Analysis

WORK EXPERIENCE

Internship Trainee
127kV Grid Station, Mianwali

08/2023 - 10/2023 *Mianwali, Pakistan*

Faisalabad Electric Supply Company (WAPDA) at 127kV Grid Station

Achievements/Tasks

- Practiced in backup power management for uninterrupted operations in case of faults detection
- Consummate cooling operation system of transformer
- Perceived functioning of International grid system of Pakistan

Contact : Sanaullah Khan - 0459-920190

Artificial Intelligence Trainee Remote
Info aidTech

05/2023 - 06/2023 *Kalimpong, India*

IT Services and IT Consulting company in India

Tasks

- Created a Chatbot using the NLTK library
- Implemented Voice Recognition using the speech recognition library
- Implemented Sentiment Analyzer using the VADER from the NLTK library

ORGANIZATIONS

Namal Media Club (11/2023 - Present)
Vice President

Skills Development Society, Namal (07/2022 - 09/2023)
Functional Manager

SKILLS

Verilog | VHDL | C | C++ | Matlab | System Verilog | Cadence | Verilator | Qflow | Modelsim | Linux | Assembly Language | Magic | Xilinx ISE

UNDERGRADUATE PROJECTS

Design and Integration of Branch Predictors in CV32E40P RISC-V core (10/2023 - Present)

- Designed 2-bit and two-level branch predictors for CV32E40P core to increase its performance.
- Integrated the 2-bit and two-level branch predictors in CV32E40P core.
- Analyzed that after the integration of 2-bit and two-level branch predictors clock cycles reduced and performance of the CV32E40P core increased for different benchmarks.

RISC-V Pipelined Single Cycle Processor (10/2023 - 01/2024)

- Designed a RISC-V pipelined single cycle processor using verilog language

CERTIFICATES

IC chip Designing (07/2022 - 02/2022)
I learned Linux and Verilog during training, inspiring me to explore and improve my skills in open source field.

Associate Membership (09/2023 - Present)
I am the associate member of Pakistan Nuclear Society which has the objective to promote peaceful uses of nuclear technology.

LANGUAGES

English
Full Professional Proficiency

Urdu
Native or Bilingual Proficiency

INTERESTS

Semiconductors | VLSI | SOC | RTL | FPGA | Embedded Systems