# Muhammad Farhan
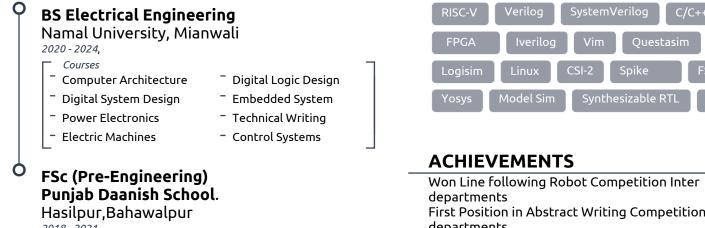## Electrical Engineer

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Hasilpur, Bahawalpur, Pakistan

Visit My Linkedin Profile

I am a passionate Electrical engineer at Namal University Mianwali, eager to embark on a career in Hardware Design and Verification. I have a strong understanding of SoC design, ASIC implementation, and RISC-V architecture, and I am driven to translate theoretical knowledge into practical applications, contributing effectively and innovatively to cutting-edge projects.

## EDUCATION

### BS Electrical Engineering
Namal University, Mianwali
*2020 - 2024,*

Courses
- Computer Architecture
- Digital System Design
- Power Electronics
- Electric Machines
- Digital Logic Design
- Embedded System
- Technical Writing
- Control Systems

### FSc (Pre-Engineering)
### Punjab Daanish School.
Hasilpur,Bahawalpur
*2018 - 2021*

## PERSONAL PROJECTS

RISC-V Single Cycle and Pipelined Processor Design
- From single cycle to pipelined processor without hazard detection logic

4-bit ALU Design and Hardware Implementation
- I designed and implemented a 4-bit Arithmetic Logic Unit (ALU) capable of performing basic arithmetic and logical operations such as addition, subtraction, AND, OR, and XOR.

System Verilog Layered Testbench Project
1. **4-bit Adder (sequential, Combinational)**
2. **FIFO**
3. **D-Flip Flop**

## WORK EXPERIENCE

### RTL Training and Linux Fundamentals
CESD-Namal, 10XEngineers

*CESD-Namal University*

Achievements/Tasks
- Learned Hardware Description Languages (HDL) including Verilog, SystemVerilog and UVM .
- Practiced HDL languages and learned basic Linux commands.

### Ex: IEEE Marketing Director
IEEE-NSB
*04/2022 - 08/2022,*  *IEEE Namal Student Branch*

Achievements/Tasks
- As the marketing head for IEEE at Namal University, I promote the organization's activities

## SKILLS

RISC-V | Verilog | SystemVerilog | C/C++
FPGA | Iverilog | Vim | Questasim
Logisim | Linux | CSI-2 | Spike | FSM
Yosys | Model Sim | Synthesizable RTL | UVM

## ACHIEVEMENTS

Won Line following Robot Competition Inter departments
First Position in Abstract Writing Competition Inter departments

## CURRENT PROJECT FYP

**Functional Verification of MIPI (Mobile Industrial Processor Interface) Using UVM (Universal Verification Methodology) In QuestaSim**

## ORGANIZATIONS

IEEE (Namal Student Branch) (04/2022 - 08/2022)

NSSI(Namal Society for Social Impact)
(03/2022 - 06/2022)

## CERTIFICATES

RTL Design and Verification (07/2023 - 09/2023)
*Center of Excellence and Skills Development*

Verilog HDL Fundamentals for Digital Design and Verification (04/2024)
*Udemy*

## LANGUAGES

English
*Full Professional Proficiency*

Urdu
*Full Professional Proficiency*

## INTERESTS

Hardware Design and Verification | SoC Design